## Perspective on the Future Electronics Based on Two-Dimensional Materials

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With the dimension scaling in dimension, the transistor gate controllability becomes weaker owing to the pronounced source-drain tunneling. Hence, the transistor body thickness needs to be reduced to ensure efficient electrostatic control. New materials such as "ultra-thin" 2D semiconducting materials have attracted attention. In this talk, I would like to provide analysis and arguments on the possibility to scale the device dimension, for example down to 1nm technology node or beyond, using 2D transition metal dichalcogenides (TMD) semiconductors. The benchmark of 2D semiconductors and Si at various technology nodes shall also be briefed.

There are many challenges on device fabrication. Here, I would like to discuss on several major bottlenecks and the advancements we and collaborators have achieved recently. (1) We discover that hydroxide vapor phase epitaxy enables the growth of WS<sub>2</sub> monolayers with a significantly lower density of structural defects, which make the electron mobility peaked at ~200 cm<sup>2</sup>/Vs. (2) The mechanism of wafer-scale growth of 2D materials will also be discussed. (3) Ultrahigh-k dielectrics can be applied onto short-channel (<30 nm) 2D monolayer transistors to greatly lower the subthreshold swing (down to 70 mV dec<sup>-1</sup>) with an ON/OFF current ratio up to 10<sup>7</sup>. (4) Semimetal is a feasible n-type contact metal to TMD monolayers that can achieve almost zero SB height. Many other unresolved challenges shall also be discussed.

## **Speaker Biography:**

## Lain-Jong Li (Lance Li)

Current position:

Professor, Chair of Future Electronics & Chair of Physics by Courtesy Department of Mechanical Engineering, The University of Hong Kong

Education:

- BA (1994) and MSc (1996) of Chemistry, National Taiwan University
- D.Phil (2006) of Condensed Matter Physics, Oxford University.

Publication Record:

- Highly cited scholar: 2018, 2019, 2020, 2021, 2022 (Clarivate)
- Published over 430 referred papers (50865 citations; H-index of 106)(Web of science)

Experience:

- Assistant Professor, MSE, NTU (Singapore) Jun 2006 Dec 2009
- Associate Research Fellow, Academia Sinica (Taiwan) / Feb 2010 Apr 2014
- Research Fellow (Tenured), Academia Sinica (Taiwan) / May 2014 Jul 2014
- Associate Professor, King Abdullah University of Science and Technology (Saudi Arabia) / Aug 2014 – Jul 2016
- Full Professor, King Abdullah University of Science and Technology (Saudi Arabia) / Aug 2016 Dec2017
- Chief Technology Officer (CTO), Nitronix Nanotechnology, Taiwan 2015- Dec 2017
- SHARP Professor (adjunct), University of New South Wales (Australia) / Sep2018-Dec 2020
- Director, Corporate Research in Taiwan Semiconductor Manufacturing Company (Taiwan)/Dec2017-Dec2020

## **Research** interests

Two-dimensional materials hold tremendous promises in replacing current silicon-based technology for manufacturing compact and low-energy-consuming nanoelectronics. However, few major bottlenecks (growth, device contact/geometry, 3D integration approach) need to be overcome. He focuses on solving these challenges for advancing manufacturing and extending the Moore's Law for future electronics.

